Amendments to the Claims

This listing of claim will replace all prior versions and listings of claim in the application.

1-53. (canceled)

54. (previously presented) A method of operation in an integrated circuit memory device that includes an array of memory cells, wherein the method comprises:

receiving an external clock signal;

receiving information that specifies that the memory device perform a memory write operation;

in response to the information, receiving a first data value after a time gap;

receiving a second data value after receiving the first data value, wherein the first and second data values are received using a set of pins;

receiving a first mask bit and a second mask bit, wherein the first and second mask bits are received in succession during a clock cycle of the external clock signal using a pin on the memory device, wherein the first mask bit indicates whether to write the first data value to the array during the memory write operation and the second mask bit indicates whether to write the second data value to the array during the memory write operation.

55. (previously presented) The method of claim 54, wherein:

when the first mask bit indicates that the first data value is to be written to the array, writing the first data value to the array during the memory write operation; and

when the second mask bit indicates that the second data is to be written to the array, writing the second data value to the array during the memory write operation.

56. (previously presented) The method of claim 54, further including:

receiving a plurality of control signals that specify that the memory device perform a row sensing operation; and

during the row sensing operation, sensing a row of the array of memory cells.

57. (currently amended) The method of claim 56, wherein:

~~if~~ when the first mask bit indicates that the first data value is to be written, writing the first data value to a first memory location in the row of memory cells; and

~~if~~ when the second mask bit indicates that the second data value is to be written, writing the second data value to a second memory location in the row of memory cells.

58. (previously presented) The method of claim 57, wherein the first memory location is identified by a column address.

59. (previously presented) The method of claim 54, wherein the memory device is a dynamic random access memory device.

60. (previously presented) The method of claim 54, further including receiving error detection and correction information on the pin.

61. (previously presented) The memory device of claim 54, wherein the information also specifies whether to precharge a plurality of sense amplifiers used in writing at least one of the first and second data values to the array.

62. (previously presented) The method of claim 61, wherein a first control value is encoded in the information to specify that the precharge operation is performed automatically following the memory write operation.

63. (previously presented) The method of claim 54, wherein the information is included in a request packet, wherein receiving the information further comprises receiving the request packet using the set of pins.

64. (previously presented) The method of claim 63, wherein the request packet includes a third mask bit and address information, wherein the third mask bit indicates whether to write a third data value to the array of memory cells.

65. (previously presented) The method of claim 64, further including receiving the third data value before receiving the first data value.

66. (previously presented) The method of claim 54, wherein:

the first data value is received during a first half of the clock cycle of the external clock signal; and

the second data value is received during a second half of the clock cycle of the external clock signal.

67. (previously presented) The method of claim 54, further including:

receiving a third mask bit along with the first data value, wherein the third mask bit indicates whether to write a third data value to the array; and

receiving a fourth mask bit along with the second data value wherein the fourth mask bit indicates whether to write a fourth data value to the array.

68. (previously presented) The method of claim 54, wherein the pin is not included in the set of pins.

69. (previously presented) A semiconductor memory device that includes an array of memory cells, wherein the memory device comprises:

a set of interface terminals to receive information which specifies that, after a time gap, the memory device receive a first set of data bits followed by a second set of data bits; and

a terminal to receive;

a first mask bit during a first half of a clock cycle of an external clock signal, the first mask bit indicating whether the first set of data bits is to be written to the array; and

a second mask bit during a second half of the clock cycle of the external clock signal, the second mask bit indicating whether the second set of data bits is to be written to the array.

70. (previously presented) The memory device of claim 69, wherein the memory cells are dynamic random access memory cells.

71. (currently amended) The memory device of claim 69, wherein the memory device receives error detection and correction information on the ~~dedicated~~ terminal.

72. (previously presented) The memory device of claim 69, wherein:
the first set of data bits is received at a time offset from receipt of the first mask bit; and
the second set of data bits is received at a time offset from receipt of the second mask bit.

73. (previously presented) The memory device of claim 69, further including a plurality of pins to receive the first set of data bits and the second set of data bits from a set of external signal lines.

74. (previously presented) The memory device of claim 69, wherein:
the first and second mask bits are received during a first clock cycle of the external clock signal;
the first set of data bits is received during a first half of a second clock cycle of the external clock signal; and
the second set of data bits is received during a second half of the second clock cycle of the external clock signal.

75. (previously presented) The memory device of claim 69, further including a plurality of pins, coupled to the set of interface terminals, to receive the information.

76. (previously presented) The memory device of claim 69, wherein both the first set of data bits and the second set of data bits are received on the set of interface terminals.

77. (previously presented) The memory device of claim 69, wherein the information is received during a first clock cycle of the external clock signal, and the first and second sets of data bits are received during a second clock cycle of the external clock signal.

78. (currently amended) The memory device of claim 69, wherein the terminal also receives a data bit, wherein the first mask bit, the second mask bit and the data bit are received by the ~~dedicated~~ terminal in a multiplexed format.

79. (previously presented) The memory device of claim 69, further including a set of pins to receive the first and second sets of data bits in succession during a clock cycle of the external clock signal.

80. (previously presented) The memory device of claim 69, wherein the information is included in a request packet.

81. (previously presented) The memory device of claim 80, wherein the request packet includes a third mask bit, a fourth mask bit and address information.

82. (previously presented) The memory device of claim 81, wherein:
the third mask bit indicates whether a third set of data bits is to be written to the array; and
the fourth mask bit indicates whether a fourth set of data bits is to be written to the array.

83. (previously presented) The memory device of claim 82, wherein the third and fourth mask bits are received using the set of interface terminals.

84. (previously presented) A method of controlling a semiconductor memory device, wherein the memory device includes an array of memory cells, wherein the method comprises:
providing a first control value to the memory device that indicates that the memory device, after a time gap, receive a first set of data bits and a second set of data bits;

after the time gap and during a first half of a clock cycle of an external clock signal, providing a first mask bit to the memory device, wherein the first mask bit indicates whether to write the first set of data bits to the array; and

during a second half of the clock cycle of the external clock signal, providing a second mask bit to the memory device, wherein the second mask bit indicates whether to write the second set of data bits to the array.

85. (previously presented) The method of claim 84, wherein providing the first control value further comprises encoding the first control value to indicate whether the memory device should precharge sense amplifiers used in writing at least one of the first and second sets of data bits to the array.

86. (previously presented) The method of claim 84, further including:

providing the first set of data bits to the memory device; and

providing the second set of data bits to the memory device.

87. (previously presented) The method of claim 84, further including providing information to the memory device that instructs the memory device to ignore the first and second mask bits.

88. (previously presented) The method of claim 87, further including providing a control signal to the memory device that causes the information to be stored in a register on the memory device.

89. (previously presented) The method of claim 84, wherein providing the first and second mask bits to the memory device further comprises providing the first and second mask bits to the memory device over a single signal line.

90. (previously presented) The method of claim 84, further including providing a second control value to the memory device, wherein the second control value indicates that the memory device is to transfer data stored in a row of the array of memory cells to a row of sense amplifiers.

91. (previously presented) The method of claim 84, further including:

providing a third mask bit to the memory device, wherein the third mask bit is provided concurrently with the first set of data bits and indicates whether to write a third set of data bits to the array;

providing a fourth mask bit to the memory device, wherein the fourth mask bit is provided concurrently with the second set of data bits and indicates whether to write a fourth set of data bits to the array.

92. (previously presented) The method of claim 91, further including:

providing the first and second sets of data bits to the memory device during a first clock cycle of the external clock signal; and

providing the third and fourth sets of data bits to the memory device during a second clock cycle of the external clock signal.

93. (previously presented) The method of claim 84, wherein providing the control value further comprises providing a request packet that includes the control value.

94. (previously presented) A semiconductor memory device, comprising:

an array of memory cells;

a plurality of pins to receive control information that specifies that, after a time gap, the memory device receive data; and

an input pin to receive:

a first mask bit during a first half of a clock cycle of an external clock signal, wherein the first mask bit indicates whether to write a first portion of the data to the array; and

a second mask bit during a second half of the clock cycle of the external clock signal, wherein the second mask bit indicates whether to write a second portion of the data to the array.

95. (previously presented) The memory device of claim 94, further including a plurality of pins to receive the data.

96. (previously presented) The memory device of claim 94, wherein the array of memory cells includes dynamic random access memory cells.

97. (previously presented) The memory device of claim 94, wherein the input pin further receives a bit of data, and wherein the first mask bit, the second mask bit and the bit of data are received from the input pin in a multiplexed format.

98. (previously presented) The memory device of claim 94, wherein the control information is included in a request packet.

99. (previously presented) A semiconductor memory device including an array of memory cells, wherein the memory device comprises:

means for receiving a first data value and a second data value;

means for receiving:

a first mask bit that indicates whether to write the first data value to the array during an internal memory write operation; and

a second mask bit that indicates whether to write the second data value to the array during the internal memory write operation,

wherein the first and second mask bits are received during a clock cycle of an external clock signal.